PERFORMANCE ANALYSIS OF NANO ELECTRONIC SINGLE ELECTRON TRANSISTOR BASED 8-BIT A/D CONVERTERS

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ABSTRACT

A thorough study on the performance of eight bit Analog-Digital converters based on single electron transistors has been done in this paper. The Single Electron Transistors are smaller in size, operate at a greater speed and have low power consumption when compared to CMOS. Three methods of Analog to Digital Conversion techniques Complementary Single Electron Tunnelling Transistor, Periodic Symmetric Function, SET/MOS hybrid using Single Electron Transistor have been discussed for Eight bit operation. A comparison of these methods quantitatively and qualitatively has also been presented.

Keywords: *analog-digital conversion, metal-oxide-semiconductor, nano electronics, ULSI, single-electron transistor, SPICE.*

INTRODUCTION

The ultimatum of current trends in the surface of designers in the field of electronics in size is the major challenge to appeal and for integration [1]. In the process of continuing implementation in the miniaturization of integrated circuits, it is possible that the present micron-scale measures will be replaced with nanometer scale. Nano electronics is an advanced innovation in technology where few electrons are sufficient to define a logic state instead of that defined by millions of electrons in the ongoing trends defining CMOS [2] technology.

Single electron transistor, which is a nano device, provides excellent potential for future Ultra Large Scale Intyegrated(ULSI) circuits due to the reasoning for low power consumption and size scalability integration [3]. Moreover, the analog and digital converters are essential trunk of system-on-chip (SOC) products as it bridges the gap between the analog physical construct and the digital logical construct.

A single-electron transistor [4-8] consists of a small conducting island coupled with source and drain, leads by tunnel junctions, and capacitively coupled to one or more gates. The symbol of a SET is shown in Fig. 1 and the equivalent electrical circuit is shown in Fig. 2. The voltage of the island is the function of number of electrons on the island

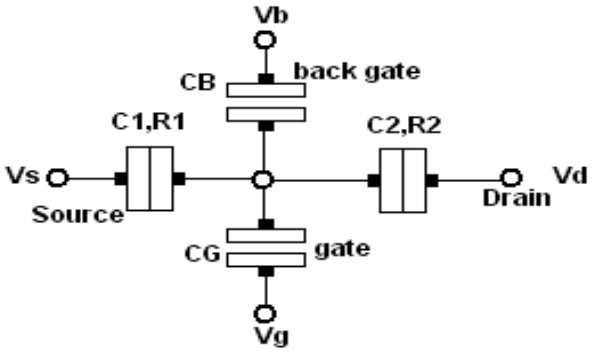

Figure 1: SET Symbol

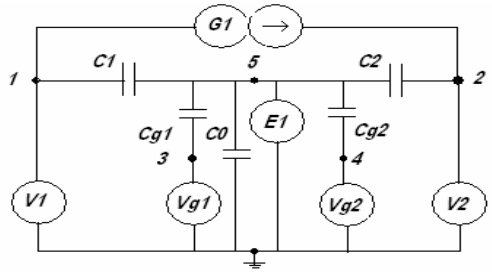

Figure 2: SET Equivalent Circuit

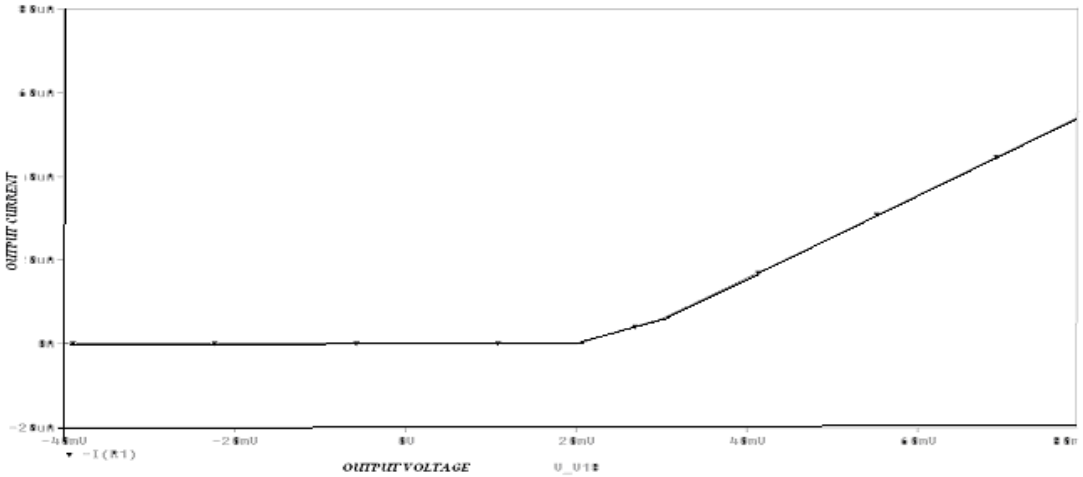

Figure 3: V- I Characteristics

The V-I Characteristics of the SET is shown in fig: 3. The zero part of the curve indicates coulomb blockade where no tunneling takes place and as the bias voltage is applied, the electrons tunnel through the island from the source to the drain. Analog and digital signal conversion is necessary in modern signal processing systems. The development of ULSI circuits promotes the analog–digital conversion (ADC) to develop in the direction of high integration density, high speed, and low power dissipation[9-10]. The ADC circuits based on the single-electron transistor (SET) have the potential advantages of high integration density, low power dissipation, and high speed. This paper analyses three novel schemes for obtaining high resolution, high speed and low power ADC circuits. Some research groups have proposed several kinds of ADC and DAC circuits based on SET [16,22].Xiaobin Ou and Nan-Jian Wu [16] have presented A/D conversion and D/A conversion that consists of SET and MOS hybrid circuits. They have simulated 3-bit ADC and 2-bit DAC.Hiroshi Inokawa [12] has proposed merged SET and MOS devices that serve as a universal literal gate and quantizer. Based on the universal literal gate they have discussed its application to A/D conversion. C.H. Hu, S.D Cotofana [20] have presented a D/A conversion circuit based on (SETT) Single Electron Tunneling Transistor that fully utilizes the coulomb blockade effect.

The ADC and DAC circuits consist of single-electron junctions, SETs, and turnstile circuits. Though they have shown good conversion characteristics and much low power dissipation, there are some common problems that the load capability and signal swing of the ADC circuits for higher bit operation are too small, it is difficult to use them in practice. This paper discusses some issues related to the resolution, the operating speed and the power dissipation of the ADC circuits and contributes only to the performance analysis for advancing the implementation of A/D conversion circuits using SET for eight bit operations. The SPICE macro-modeling [11,13,14]of the SET is used for simulating ADC circuits. Finally, the main results are summarized

A/D CONVERTER CIRCUIT USING CSET

A.Complementary Single Electron Tunneling Transistor

The schematic shown in Fig: 4 is known as the Tucker inverter. According to [19] it is possible to get a square-wavelike output signal having about 50% duty ratio. In the first half period, when q_{out}=e in the initial state, the

lower SETT will turn on and one electron is transported to the ground and the transportation of more electrons is prohibited by the coulomb blockade. When q_{out} =0, the output will be kept stable by the coulomb blockade. In the other half period, when q_{out} =0 in the initial state, the upper SETT will turn on and one electron is transported to output capacitor and the transportation of more electrons is prohibited by the coulomb blockade. Thus a square wave output

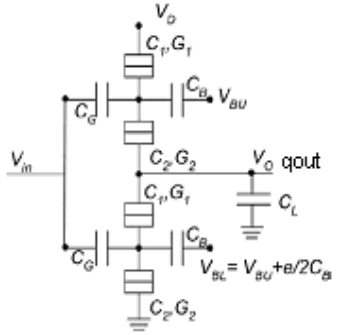

Figure 4: Schematic of CSETT

with 50% duty ratio is obtained. According to [9], the boundaries between stability and instability for '0'K approximations of CSETT are as follows:

$$-e\,(n+1/2) + q_0 = C_G\,(V_D - V_G) + C_2 V_D + C_B\,(V_D - V_B) \quad (1)$$

$$e\,(n-1/2) - q_0 = C_G(V_D - V_G) - C_2 V_D + C_B(V_D - V_B) \quad (2)$$

$$e\,(n-1/2) - q_{0=} C_G V_G + C_1 V_D + C_B V_B \quad (3)$$

$$-e\,(n+1/2) + q_{0=} -C_G V_G - C_1 V_D - C_B V_B \quad (4)$$

where, C1-Capacitance of the tunnel junction 1 in aF,C2- Capacitance of the tunnel junction 2 in aF, q_0-Random background charge,C_G - Capacitance of the gate terminal in aF,C_B- Capacitance of the back gate in aF, V_G-Gate input voltage, V_B - Back gate voltage,V_D - Drain voltage, e- electronic charge and n- number of electrons.

On solving the upper SETT boundary conditions for n=0, from equations (2) and (4) we obtain,

$$V_D = \frac{e}{2(C_G + C_B + C_1 + C_2)} \quad (5)$$

$$V_D = \frac{-C_G V_G}{C_1} + \frac{e}{2C_1} \quad (6)$$

Then to keep the upper SETT closed in one half period and open in the other half period when the V_{DS} keeps constant, V_D has to be set as follows:

$$V_D = \frac{e}{2(C_G + C_B + C_1 + C_2)} = \frac{-C_G(V_G + e/2C_G)}{C_1} + \frac{e}{2C_1} \quad (7)$$

where, C1-Capacitance of the tunnel junction 1 in aF, C2- Capacitance of the tunnel junction 2 in aF, C_G - Capacitance of the gate terminal in aF,C_B- Capacitance of the back gate in aF, V_G- Gate input voltage, V_D - Drain voltage and e- electronic charge.By solving the equation (7) we get

$$V_D = \frac{e}{2(C_G + C_B + C_1 + C_2)} \quad (8)$$

For the lower SETT, $V_D \approx e/C_L$

So, $$CL = e/VD = 2(CG + CB + C1 + C2) \quad (9)$$

Based on the CSETTs (Complementary Single Electron Tunneling Transistor) structure [9], an n bit ADC architecture as depicted in Fig. 5 It consists of a capacitive divider and n pairs of complementary SETTs.

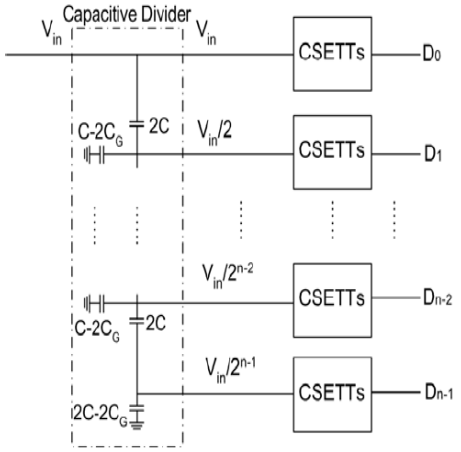

Figure 5: Architecture of ADC

First, the input signal Vin is divided into Vin/2i, i =0, 1, 2 … n-1, by the capacitive divider, then it is encoded into the corresponding binary output signals by the CSETTs.

Table 1: 8-bit ADC using CSETT-analog input and digital output

Input voltage in mV	Digital output voltage							
	D7	D6	D5	D4	D3	D2	D1	D0
0- 5.07	0	0	0	0	0	0	0	0
5.08 - 10.16	0	0	0	0	0	0	0	1
10.26 - 15.24	0	0	0	0	0	0	1	0
20.3 - 25.35	0	0	0	0	0	1	0	0
40.6 - 45.63	0	0	0	0	1	0	0	0
81.2 - 86.19	0	0	0	1	0	0	0	0
162.24 - 167.31	0	0	1	0	0	0	0	0
324.48 - 329.55	0	1	0	0	0	0	0	0
648.96 - 654.03	1	0	0	0	0	0	0	0
1293 - 1297.92	1	1	1	1	1	1	1	1

B. SIMULATION RESULTS OF ADC CIRCUIT USING CSETT

The simulation results for 8-bit CSETT ADC have been obtained in Spice Software, the macro model for the CSETT block has been used to simulate the results.. In Fig.6 the first waveform is the input ramp voltage, the rest of the waveform show the output D0, D1, D2, D3, D4, D5, D6 and D7. The input voltage is 1. 3V, so the Resolution is 1.3/256=5.07mv. The tabulation of the input ramp voltage and the digital output voltage is shown in Table I.

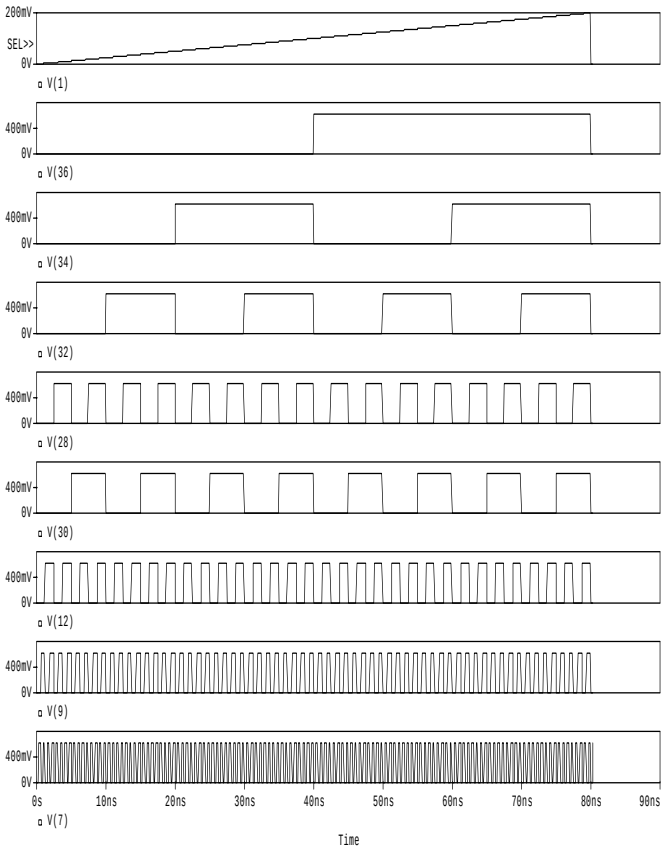

Figure 6: Simulation results of 8 –bit CSETT- ADC

A/D CONVERSION USING PSF (PERIODIC SYMMETRIC FUNCTION)

A. PERIODIC SYMMETRIC FUNCTION

A Periodic Symmetric Function (PSF) Fp(x) is a symmetric function for which Fp(x) = Fp(x+T), where T is the period. Any PSF can be completely characterized by T, the value of its period, and a, b, the values of X corresponding with the first positive transition and the first negative transition, as displayed in Fig.7 Given the periodic transfer function of the SET transistor, we can design a PSF block that can compute any PSF[21] using a single SET transistor as a basis. The period of the SET transistor's transfer function can be adjusted to T by varying the value of the gate capacitor Cg. Likewise, the drain-source voltage Vds determines the part of the function period in which Id > 0 i.e., the length of the [a, b] interval. Finally, a coactively coupled bias voltage similar to that used for the CMOS-type inverter can translate the transfer function over the X axis in order to place the [a, b] intervals in the required positions.

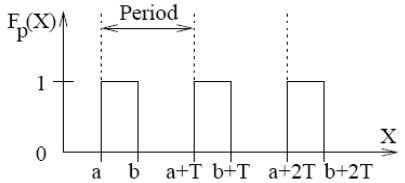

Figure 7: Periodic Symmetric Function Fp(x)

A PSF block can be implemented using a SET electron trap (Cc and Cj) in combination with a SET inverter Fig.10 The electron trap has a triangular periodic transfer function. The electron trap and the transfer function are shown in Fig 8 and Fig.9 respectively. The inverter, in this case, acts as a literal gate and transforms the triangular transfer function into a rectangular shape.

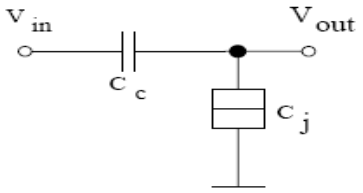

Figure 8: Electron trap

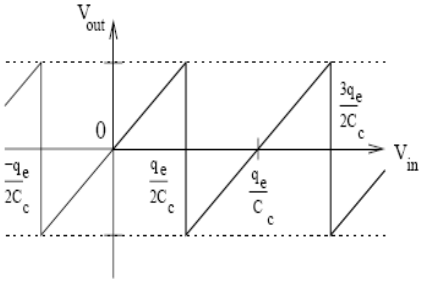

Figure 9: Electron trap - periodic transfer function

The SET inverter behaves as a literal gate and transforms its input signal (within a limited range) to either logic '0' or logic '1'. The inverter is modified such that it has two inputs.

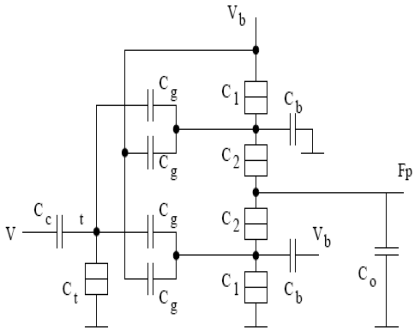

Figure 10: PSF block

One of its inputs is attached to a bias voltage Vb. The bias voltage is set such that the inverter is close to its switching point. The output of the electron trap serves as the second input to the modified inverter block. If the output of the electron trap is negative, the inverter interprets the combined input of the electron trap and the bias voltage as logic '0' and its output becomes '1'. Likewise, if the output of the electron trap is positive, the inverter interprets the combined input of the electron trap and the bias voltage as logic '1' and its output becomes '0'. According to [12] V = qe/αC, a = qe/αC, b = e/αC and T = 2qe/αC. Assuming α = 100 we find Cc = 50C. The maximum amplitude of the electron trap is determined by the total capacitance attached to node t. Choosing CΣt= αC results in a maximum signal amplitude Vmax = qe/αC. The Fig.11 is a 8-bit analog to digital circuit using PSF block. The input voltage is V and the outputs are 8 binary signals d0, d1, d2, d3, d4, d5, d6 and d7. The ADC needs 8 PSF blocks designed in such a way evaluate an output signal di. For all the PSF blocks the value of b = 2a, T = 2a, and ai = 2i for di, i = 0, 1, 2…7.

B. SIMULATION RESULTS OF ADC USING PSF BLOCK

The macro model for the PSF block has been used to simulate the results. In order to increase accuracy, higher order resolution,8-bit ADCs using PSF block have been done. In Figure12 the first waveform is the ramp input voltage, the second, third, fourth, fifth, sixth, seventh, eighth and ninth waveform show the output D0, D1, D2, D3, D4, D5, D6 and D7 respectively. The input voltage is 1.6mV and the resolution (=1.6 / 256) 0.00625 mv. The tabulation of the input ramp voltage and the digital output voltage is shown in Table II

A/D CONVERSION USING SET/MOS HYBRID CIRCUIT

A. SET/MOS hybrid circuit

The schematic of a periodic literal circuit is shown in Figure 13, which consists of a SET, a MOSFET and a constant current (CC) load I_0. The SET has an input gate The MOSFET with a fixed gate bias

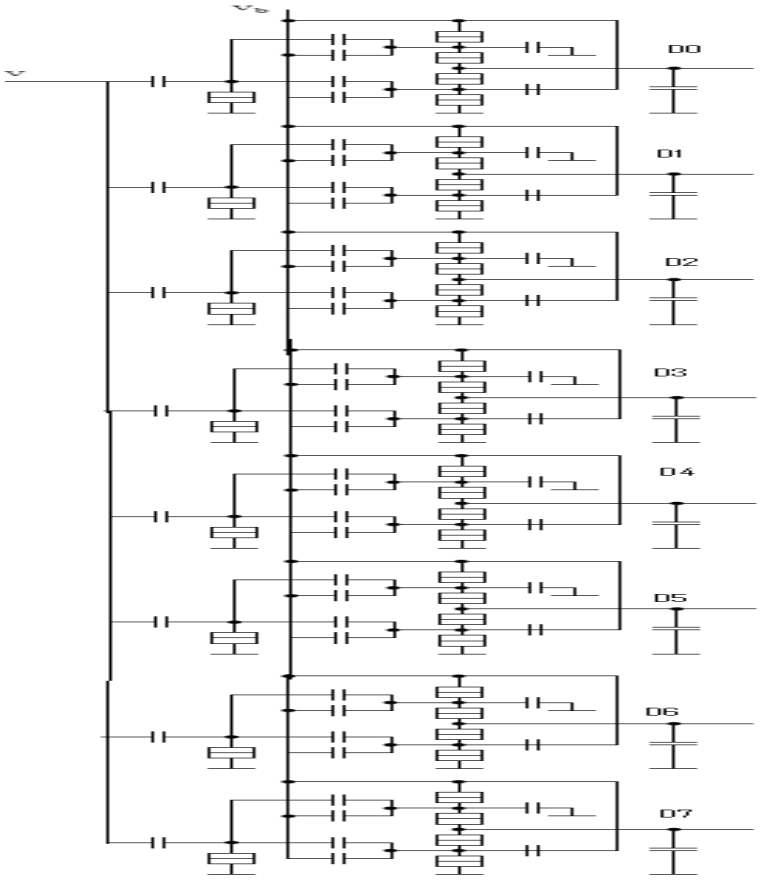

Figure 11: a 8-bit analog to digital circuit using PSF block

Table 2: 8-bit PSF-ADC analog input and digital output

Input voltage in mV	Digital output voltage							
	D7	D6	D5	D4	D3	D2	D1	D0
0- 0 . 00625	0	0	0	0	0	0	0	0
0. 00626- 0. 0125	0	0	0	0	0	0	0	1
0 . 0126 - 0.01875	0	0	0	0	0	0	1	0
0.025 - 0.03125	0	0	0	0	0	1	0	0
0. 0501-0.05625	0	0	0	0	1	0	0	0
0.101- 0.10625	0	0	0	1	0	0	0	0
0.201 - 0.20625	0	0	1	0	0	0	0	0
0.4 - 0.40625	0	1	0	0	0	0	0	0
0.8 - 0.80625	1	0	0	0	0	0	0	0
1.59375 - 1. 6	1	1	1	1	1	1	1	1

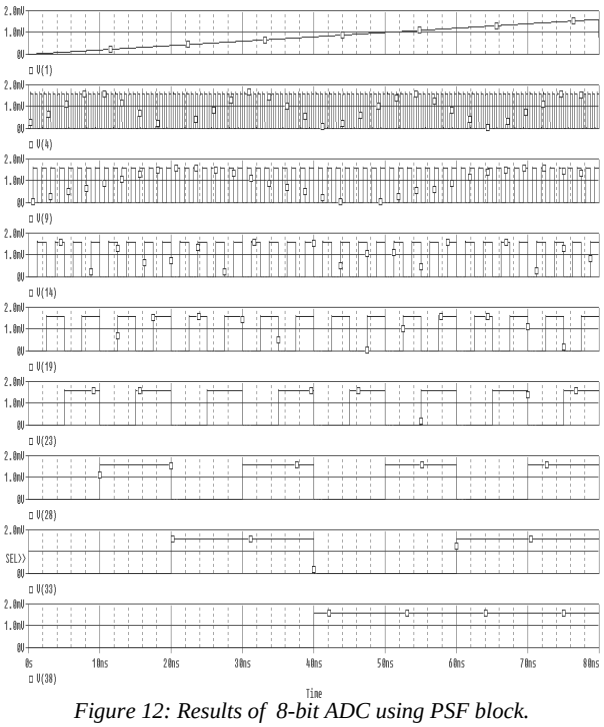

Figure 12: Results of 8-bit ADC using PSF block.

Vgg is used to keep the SET drain voltage almost constant at Vgg-Vth, Where Vth is the MOSFET threshold voltage. When CC load is connected and the increasing drain current crosses the load line of I_0, the output voltage switches from high to low. When the decreasing drain current crosses the load line, the output voltage switches from low to high value. This universal literal gate [11] is used to design the ADC.

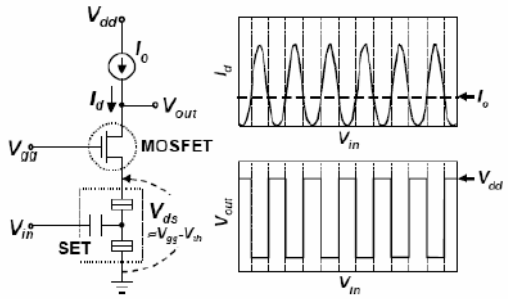

Figure 13: Schematic of Universal Literal Gate consisting of SET and MOSFET Hybrid circuit and its characteristics.

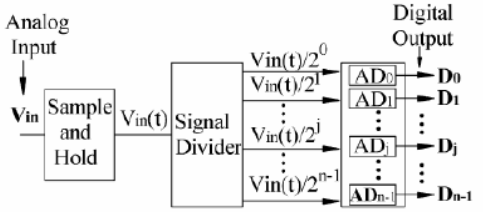

Figure 14: Basic block of ADC using SET/MOS hybrid circuit.

The block diagram of the ADC [16] using SET/MOS hybrid circuit is shown in the Fig: 14. The ADC consists of a sampling and holding circuit block (Quantizer), a signal divider circuit block, and an analog–digital signal conversion (ADC) unit block which is the universal literal gate. The sampling and hold circuit is known as the quantizer. A ramp, sinusoidal or triangular etc. input is fed at Vin and the gate of MOSFET1 is fed with short clock pulses. The transfer characteristic is obtained as shown in Fig: 17.The analog input signal is inputted to the sampling and holding circuit (Quantizer) first and then is divided by the signal divider into n signals

whose amplitudes are weighted by the ratio factors of 1/2i where i= 0,1,2,3….7. Finally, the analog signals are converted into the n-bit digital signal D0, D1, D2…D7 by the ADC circuit units.

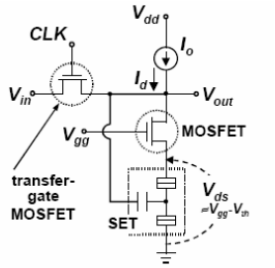

Figure 15: Quantizer

The sampling and holding circuit block consists of a MOS switch transistor and a capacitor. The signal divider block consists of a capacitor net, which produces discrete analog signals with weight coefficients1/2i, i= 0, 1, 2, 3….7. The ADC unit block consists of 8 basic universal literal gates that convert the discrete analog signals into 8-bit digital signal simultaneously.

B.SIMULATION RESULTS OF ADC USING SET/MOS HYBRID CIRCUIT

In Fig:17. the first waveform is the ramp input voltage; thesecond waveform shows the quantized output. The input voltage is 0.2V ,Vgg=1.08V and I_0=4.5nA. The parameters of SET are: C1=C2=0.18aF, Cg1=0.27aF, R1=R2=100k.

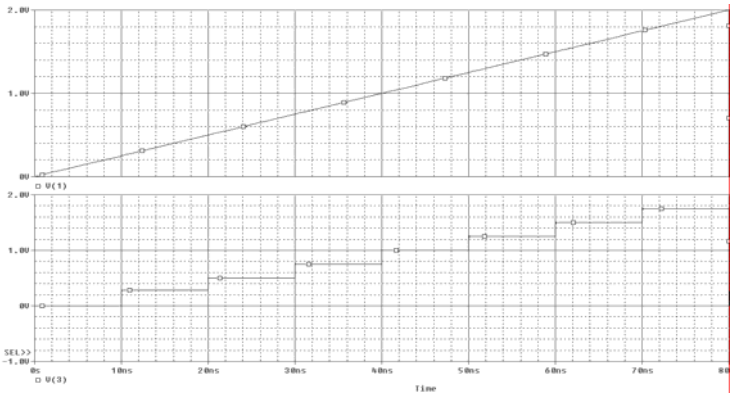

Figure 17: Quantizer output.

Table 3:8-bit ADC using SET/MOS hybrid circuit

Input voltage in mV	Digital output voltage							
	D7	D6	D5	D4	D3	D2	D1	D0
0 - 0.781	0	0	0	0	0	0	0	0
0.782 - 1.564	0	0	0	0	0	0	0	1
1.565 - 2.343	0	0	0	0	0	0	1	0
3.124 - 3.905	0	0	0	0	0	1	0	0
6.248 - 7.029	0	0	0	0	1	0	0	0
12.496 - 13.27	0	0	0	1	0	0	0	0
24.992 - 25.77	0	0	1	0	0	0	0	0
49.984 - 50.76	0	1	0	0	0	0	0	0
99.968 - 100.7	1	0	0	0	0	0	0	0
199.155 – 200	1	1	1	1	1	1	1	1

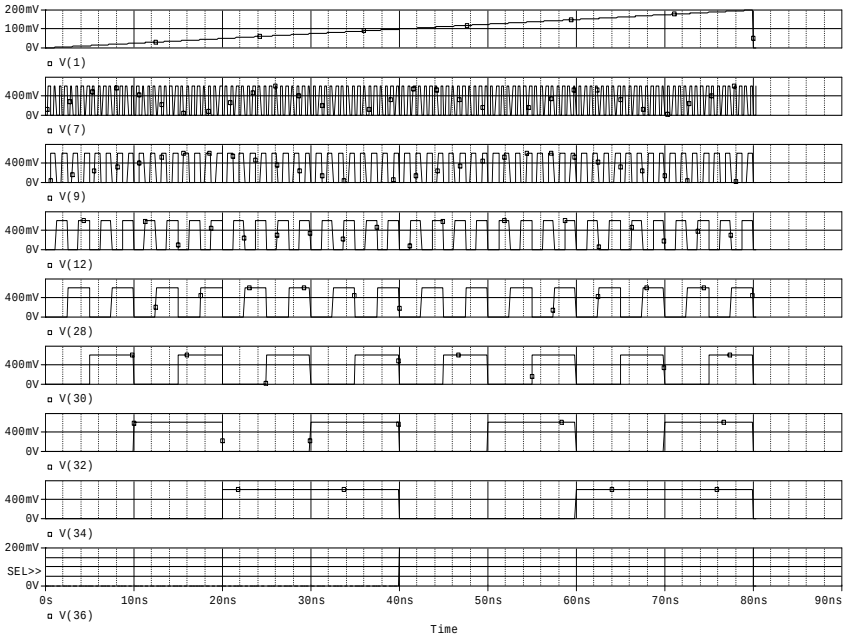

Figure 18: Response of 8-bit SET/MOS hybrid circuit

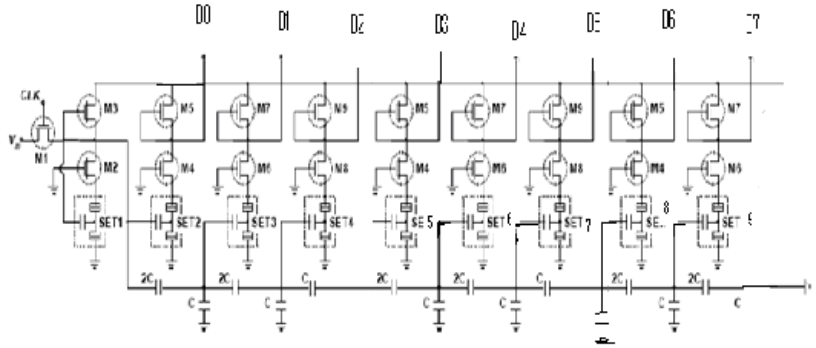

Figure 16: Schematic of 8 bit SET/MOS Hybrid circuit.

The tabulation of the input voltage and the digital output voltage is shown above in Table III. Resolution is 0.2 / 64= 0.781 mV

V PERFORMANCE COMPARISON

The comparison of ADC methods for a 8-bit conversion is presented in Table IV.The conversion rate for the ADC depends on the RC charge and discharge process. The maximal switching speed of SET circuits is determined by its RC time constant. If RT is 100k and a CTJ is 100aF. This means that the RC time constant equals 10 ps. [13]. The size, speed and power consumption of ADC using CMOS is from [9]. For an 8-bit ADC circuit realized with CMOS one would require 8^2-1 components[10] but when the ADC is realized using universal literal gate, it requires only 10 MOS transistor and 9 SET components, So the conversion rate of SET/MOS hybrid ADC is faster. But CSETT and PSF schemes employ only 16 SET Components and a few capacitors, because of this the charging and discharging time of these two ADC circuits are very less, hence conversion speed of CSETT and PSF ADC circuits are equal and faster than CMOS and SET/MOS hybrid techniques. Based on the power consumption and resolution, the PSF technique is most advantageous. One of the draw back of Single electron transistor is that it has very low gain, to compensate this SET will need to combine with MOS transistor and it appears that CMOS and SETs are rather complementary, SET has low-power consumption and has new functionality while CMOS advantages like voltage gain and input impedance.

Table 4: Comparison of ADC Methods for an 8-BIT Conversion

	CMOS	CSETT	PSF	SET/MOS Hybrid
Size	63 MOS Trans.	16 SETs and 12 Capacitors	16 SET and 8 tunnel junctions	10 MOS, 9 SET and 9 capacitor
Speed	250 MHz-1GHz	Approx. 10GHz	Approx. 10GHz	5-10GHz
Power Consumption	In range of mW	Approx. 0.6nW	Approx. 0.5nW	12 nW
Resolution	0.0195 V	5. 07 mv	0. 00625 mv	0.781 mv

CONCLUSION

In this paper, three different approaches for 8 bit ADCs based on Single Electron transistor have been analyzed. The simulation results for all the circuits have been obtained in the SPICE software using the macro model coding of SET. Quantitative and qualitative analysis have been done for the ADC methods. It is evident from the analysis and comparisons that for high resolution ADC based on SET-PSF show faster conversion rate and consume very low power hence it is the most advantageous.

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